INSTRUCTION MANUAL

Component Comparator
Type CPC 4

&

Test Limit Selector
Type TLS 1

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1.1. CPC 4 AND TLS 1 SETUP.

The CPC 4 and the TLS 1 have their own power supplies, so two mains cables are required.
Before switching-on the instruments check that the voltage selectors on the rear of both instruments have been switched to your local power line voltage (pull the switch knob, turn, and push home). The fuses should be 0.5 A or 0.3 A on CPC 4 and TLS 1 at 115 and 230 V AC respectively. Slow blow fuses should be used.
The TLS 1 is connected to the CPC 4 through a short interconnecting cable supplied with the instruments.
Then switch-on both instruments and allow abt. 20 minutes for warm-up.

1.2. CPC 4 - BASIC ADJUSTMENTS.

Set "CHECK/MEASURE" switch to "CHECK" and "CHECK 3%" in upper position.
Set range selector on 4Z1 (on left-hand module) to 3% f.s. and range selector switch on 4P1 module to 0.3% f.s. Adjust to zero on both meters using the "Adj. zero" controls.
Switch to "CHECK 3%" on 4B1 module and set "Adj. 3%" control on 4A1 for full scale deflection (3%) on 4Z1 meter.
Check that no visible deflection is obtained on $\Delta\Phi$ meter (4P1 module) when switching to "CHECK 3%". If the deflection is above $\frac{1}{2}$% of full scale, adjust pre-set control "Adj. $\Delta\Phi$" on Bridge Module 4B1 for zero deflection.

Note:

When changing measuring range on the meter modules, small zero changes will appear on the most sensitive ranges. Thus for very accurate measurements zero should always be checked on the actual range employed.

The CPC 4 is now calibrated and ready for use. To obtain best possible accuracy at high and low impedances a special calibration procedure can be used. See section 1.3.e.

1.3. CPC 4 - MEASUREMENTS.

a. Connecting Standard and Unknown

Select the required mode: R, L or C on module 4B1. The standard is connected to the upper set of coax terminals and the unknown to the lower set. The right-hand terminals detector terminals) are connected in parallel, so if desired one cable common to standard and unknown is enough.

b. Guard

When switching-on Guard, the guard-voltage, which is

following the input voltage closely, will be available on the shield of the right-hand coax terminals, and it will be available too on the guard screw terminal. So when using shielded connectors and cables the guard-voltage is automatically applied to the cable shield thereby eliminating the cable capacitance.
If the component jig or the contacting device is shielded the shield can be connected to the terminal for banana plug. When the guard switch is off, the guard terminal and connector shields are switched to instrument ground. For low impedance measurements the guard should always be switched to ground, otherwise instability may occur with impedances having an inductive component at high frequencies.

c. Measurement

The range switches for both meters are set to the required full scale ranges.
The ΔZ meter indicates the impedance difference between standard and unknown as a percentage of the standard value. The polarity signs + and -, however, are not referring to the impedance. Provided that the right mode has been selected on module 4B1 (R, L or C measurement), a positive reading will indicate that the unknown component has a higher value than the standard (Ohms, Henry or Farad).
The ΔΦ meter indicates the phase angle difference as a percentage of 1 radian. A positive reading indicates that the phase angle of the unknown is more positive than the phase angle of the standard e.g. a positive reading means:

For R:	Unknown is more inductive than standard
For L:	Unknown has higher Q than standard
For C:	Unknown has lower Q (higher losses) than standard.

NOTE: The 0.3% phase angle range cannot be used on the -50, +100% ΔZ range.

d. CHECK/MEASURE Switch

The CHECK/MEASURE switch is mainly used when calibrating the instrument.
In check position the detector input is connected to zero potential so zero adjustment of the meters is possible. When switching-on the "CHECK 3%" an error voltage corresponding to 3% deviation is applied to the detector input. The front panel switch operates a relay, which can also be operated through a rear panel socket by shorting two pins.

e. High Impedance Measurements

When measuring high impedance values errors are caused by the detector input impedance. This in series with the two measuring impedances in parallel constitutes a voltage divider so that the detector input voltage is attenuated and also suffers a phase shift depending on the ratio between the measuring impedances and the detector impedances. At 1 kHz and higher the detector impedance is mainly capacitive corresponding to about 12-15 pF with the guard switched off. With guard on this is reduced to about 5 pF. The "GUARD ON" mode is therefore normally used for all high impedance measurements, i.e. for above approx. 100 KΩ resistances or below 1000 pF capacitance.

Capacitance Measurements

When measuring capacitance values below about 200 pF the error due to input capacitance must be corrected. This may be done by connecting up two equal capacitances of the value to be measured and calibrating with the CHECK/MEASURE switch on "MEASURE". This method applies the calibrating voltage as an unbalance voltage to the generator terminals, so that the calibrating voltage is applied via the measuring impedances to the detector terminal, and any attenuation may be corrected. Capacitance values down to 10 pF may be compared accurately in this way, when employing the guard circuit.
The resistive component of the detector input impedance (about 500 MΩ) causes a phase shift when measuring low value capacitance values. This appears on the phase angle meter as a negative phase angle for a positive reading on the Z meter.
For a 10 pF measuring capacitance the error is about minus 0.1% (0.001 radian) phase angle for plus 10% capacitance reading. This error may be corrected for any given value of measuring capacitance by calibrating in the "MEASURE" position as described above and adjusting the "ΔΦ adj." pre-set control for zero deflection on the phase angle meter.

Resistance Measurement

High value resistors from about 5 MΩ to 30 MΩ may be measured accurately by the same calibration method. In this case the detector input capacitance will cause a phase shift, so that impedance deviations give rise to erroneous phase angle readings, e.g. at 30 MΩ resistance the phase angle error will be approximately half the resistance deviation. Thus accurate phase angle measurements are not practical for high resistance values except for small resistance deviations.

Shielding of Detector Leads

The guard output is connected to the shield on the detector connectors and reduces the effective shield capacitance to about 0.2%. A total shield capacitance of 250 pF corresponding to two 4 ft. coax cables thus increases the detector input capacitance by about 0.5 pF only.

Hum Interference

When measuring high impedances, some care is necessary to avoid overload due to stray hum interferences from power supply cables, etc. especially on the most sensitive ranges. The instrument should always be operated with the case grounded either via the ground lead of the supply cable or by the ground terminal on the 4A1 module. A ground connected shield adjacent to the measured component and shielded detector leads will normally give satisfactory results. Hum interference will appear as reduction of the sensitivity, or when a test limit selector is used by a wide dead band on the limit selectors.
If hum interference is suspected on any range, this may be checked by switching to the next higher range and comparing the readings.

f. Low Impedance Measurements

At low impedances the generator output is reduced due to the transformer winding resistances and leakage inductance. This is only important at the lowest impedance values, e.g. at 1 V/1 kHz an impedance of 10 Ω will reduce the generator voltage by 2%. If required this error may be corrected by calibrating with the measuring impedances connected up.
When measuring low value resistors at maximum sensitivity the leads to the measuring resistors should have equal resistance, as quite small differences will give large errors in deviation.

NOTE:

When measuring low value impedances always switch guard off to prevent instability in the input amplifier.

2.1. TLS 1 - NOTES ON SETUP.

The TLS 1 Test Limit Selector is based on the 1L1 Limit Module. Each module gives one limit adjustable within full scale deflection of the meters on the CPC 4, which again means that the position of the range switches on CPC 4 has to be considered when setting the limits. The 1L1 modules are all

identical, but they have to be coded on their PC-board according to the function in the whole setup.

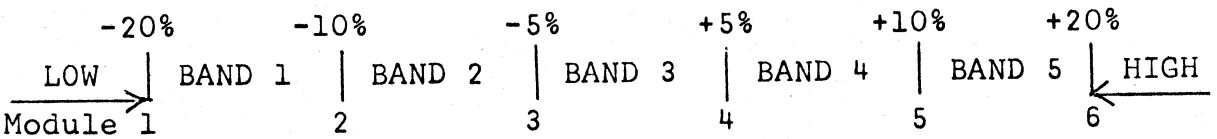
The simplest configuration is constituted by one module, which gives a GO/NO GO or below/above limit indication. A single module is often used with the CPC 4P1 module when measuring on capacitors to show whether the losses are above or below a maximum limit. A module operating alone must be coded as shown on diagram 5, LOW/HIGH $\Delta\Phi$ input (or ΔZ input).

Two modules operating together will give a LOW/PASS/HIGH indication. This setup is made by a LOW/PASS 1 and a PASS/HIGH module (diagram 5).

The above-mentioned setup with two modules is the basis, when sorting in several tolerance groups is required, e.g. LOW/2 BAND/HIGH, LOW/3 BAND/HIGH, etc., as these two modules are used for the most negative and most positive limits.

BAND - System:

Example with 6 TLS 1L1 Modules.



Module 1 : LOW/PASS 1
Modules 2, 3, 4, ... : BAND Modules
Module 6 (last module) : PASS/HIGH Refer to diagram 5 & page 9.

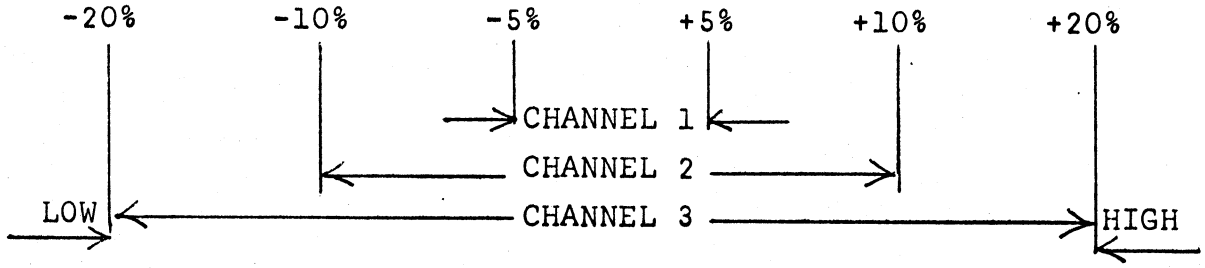
The modules must be placed side by side, but their position in the chassis is unimportant. The most negative limit should be set on the left-hand module (module 1 above), the right-hand modules being still more positive.

CHANNEL - System:

A channel system is always based on a band system with respect to the coding of the individual 1L1 modules, but additional coding must be made on a channel coding board (diagram 7), which is accessible when removing the blue cover plate. See page 11 for further details.

The center channel (channel 1) must be made by the modules in places 6 and 7 counted from the left. See overleaf.

The band system mentioned earlier as a CHANNEL system will look as follows:



2.2. TLS 1 - SETTING THE LIMITS.

First thing to do is to determine the number of limits and their values, and we consider the setup has been made according to section 2.1. above.

a. Set the range switch on module CPC 4Z1, so the most negative and the most positive limits are both within full scale deflection.
b. Turn the limit potentiometers on all 1L1 modules all the way to the right (fully clockwise).
c. Set CHECK/MEASURE switch on module CPC 4A1 to CHECK.
d. The switch on module 1S1 is set to AUTO. In this mode the TLS 1 is switching automatically between "read" and "display", i.e. no triggering is required.
e. With ADJ. ZERO potentiometer on module CPC 4Z1 an offset corresponding to the most negative limit is made.
f. Turn the limit potentiometer on module No. 1 (left-hand module) to the left (counter-clockwise) till the light shifts from the lower to the upper lamp. In the moment where the light shifts the limit is being passed, and usually a fine adjustment of the potentiometer is required to obtain the right setting. Note that there is a small hysterisis on the input, so the potentiometer can be turned slightly without shifting the light. The hysterisis is made to avoid chattering and has no practical effect on the accuracy, as a mean setting is easily obtained.
g. Proceed from e. with the next limit, i.e. adjust the meter to read the limit and adjust limit potentiometer on module No. 2 as described under f.

The same procedure as above is used for the module operating with the CPC 4P1 module simply by using the meter on this module to set the limits.

A better accuracy can be obtained by using two accurate standards for example two decade boxes, connected to the input as Standard and Unknown. The "Unknown" is set to a value for example 10% lower than nominal, and the limit potentiometer is set according to the deflection obtained on the meter. Thereby a real measurement is simulated, and the meter inaccuracy has no effect on the overall accuracy.

3.1. MANUAL COMPONENT SORTING WITH CPC 4 AND TLS 1.

The procedure will be as follows:

a. Connect unknown component.
b. Switch to MEASURE on module 4A1.
c. Reset TLS 1 with front panel TRIG button.
d. Switch to CHECK on module 4A1.
e. Remove component and put it in proper container according to TLS 1 light indication.

Comments:

b. and d. The CHECK/MEASURE switch need not to be operated, but in case a test jig is used it may be easy to open a micro-switch during the period, where the component is connected. The micro-switch should be connected between pin 1-2 and 7 on P2 on the CPC 4 rear panel. CHECK/MEASURE switch should be on MEASURE and the switch should open for measurement and close for CHECK.

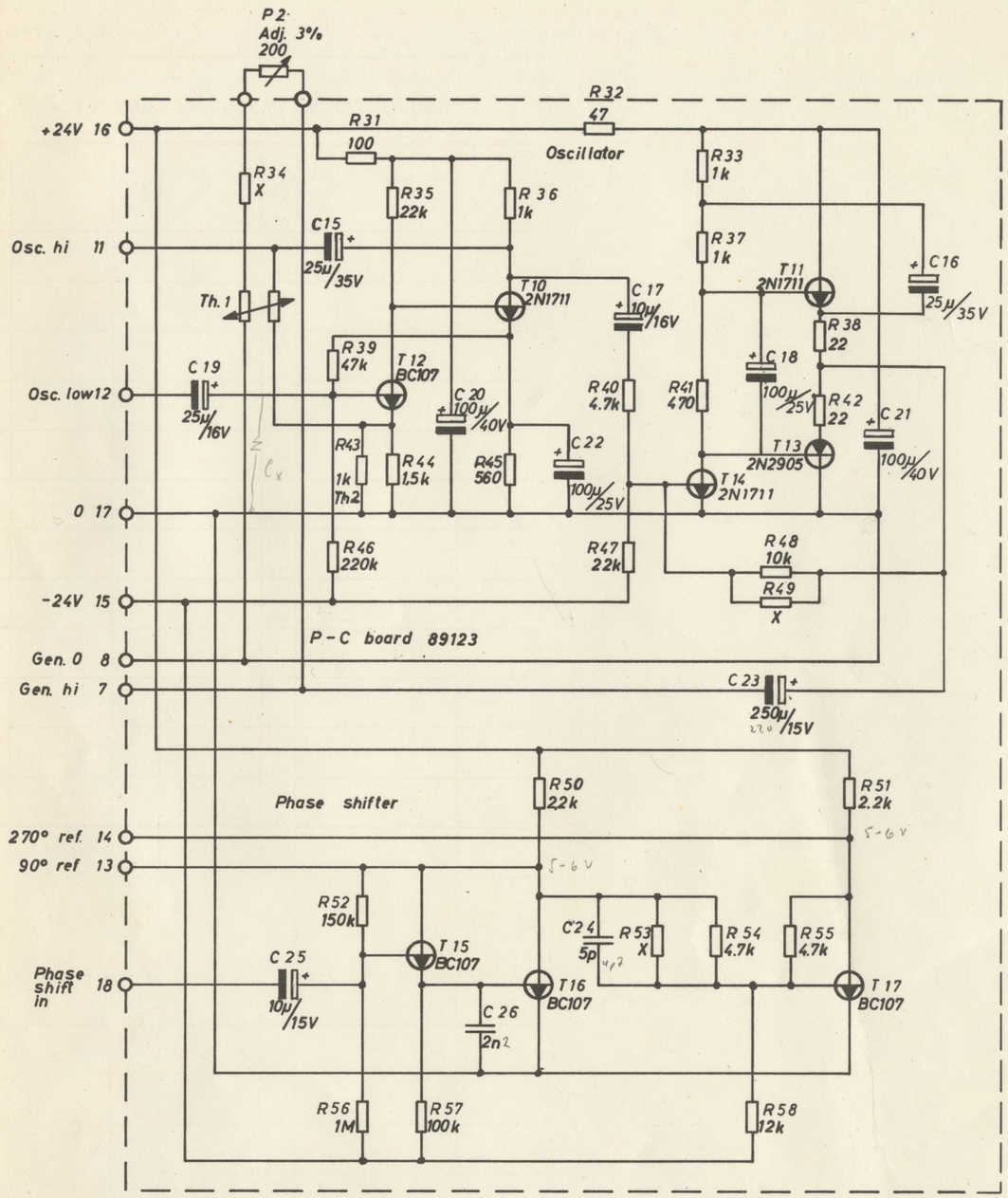
c. Pushing the TRIG button will reset the TLS 1, then it will "read" the new input and finally "display" this until reset again. Instead a contact can be connected between pins 12 and 14 on P2 on the TLS 1 rear panel. In the latter case the "read" time will be contact time plus a delay set by the DELAY potentiometer on the front panel. See page 11 for further details. The contact could be activated simultaneous to connecting the component (if a jig is used), but the delay should be set to min. 200 msec as the settling time for the analog outputs from the CPC 4 is abt. 200 msec.

NB: Both pin 12 and 14 must be kept floating with respect to TLS ground.

e. When sorting manually into several tolerance groups the output voltage (12 V AC) available on P1 on the TLS 1 rear panel can be used to drive lamps placed on the containers, where the components have to be put. (See page 10 for further details). Then the component tested must be put in the container, where the lamp is lighting, and in case a Limit Module is used on the $\Delta\Phi$ meter the reject signal from this module can be used to drive a "reject lamp".

3.2. AUTOMATIC COMPONENT SORTING WITH CPC 4 AND TLS 1.

Using sorting machines together with CPC 4 and TLS 1 is possible but no universal description of how to make the setup can be given as this has relation to the machine to a wide extent. The TLS 1 provides the signals and contact closures required to operate a machine, but usually this "information" has to be stored as the component tested only seldom is routed into the proper container immediately after the test is finished, and sometimes several test stations have to be passed before the actual sorting is made. Anyway, the TLS 1 provides the signals necessary for sorting and it can be triggered to follow the cycling of the machine - then the adaption must be made via an interface unit.



Components marked X are adjusted on test.

			061272	B.R.	
120274	B.R.		021170	B.R.	
021073	B.R.		27-5-70.	B.R.	
020773	B.R.		Rettet d.	Tegn.	Godk.

73622 0

Circuit Diagram

Component Comparator CPC-4

Module CPC-4A1

Oscillator and phase shifter

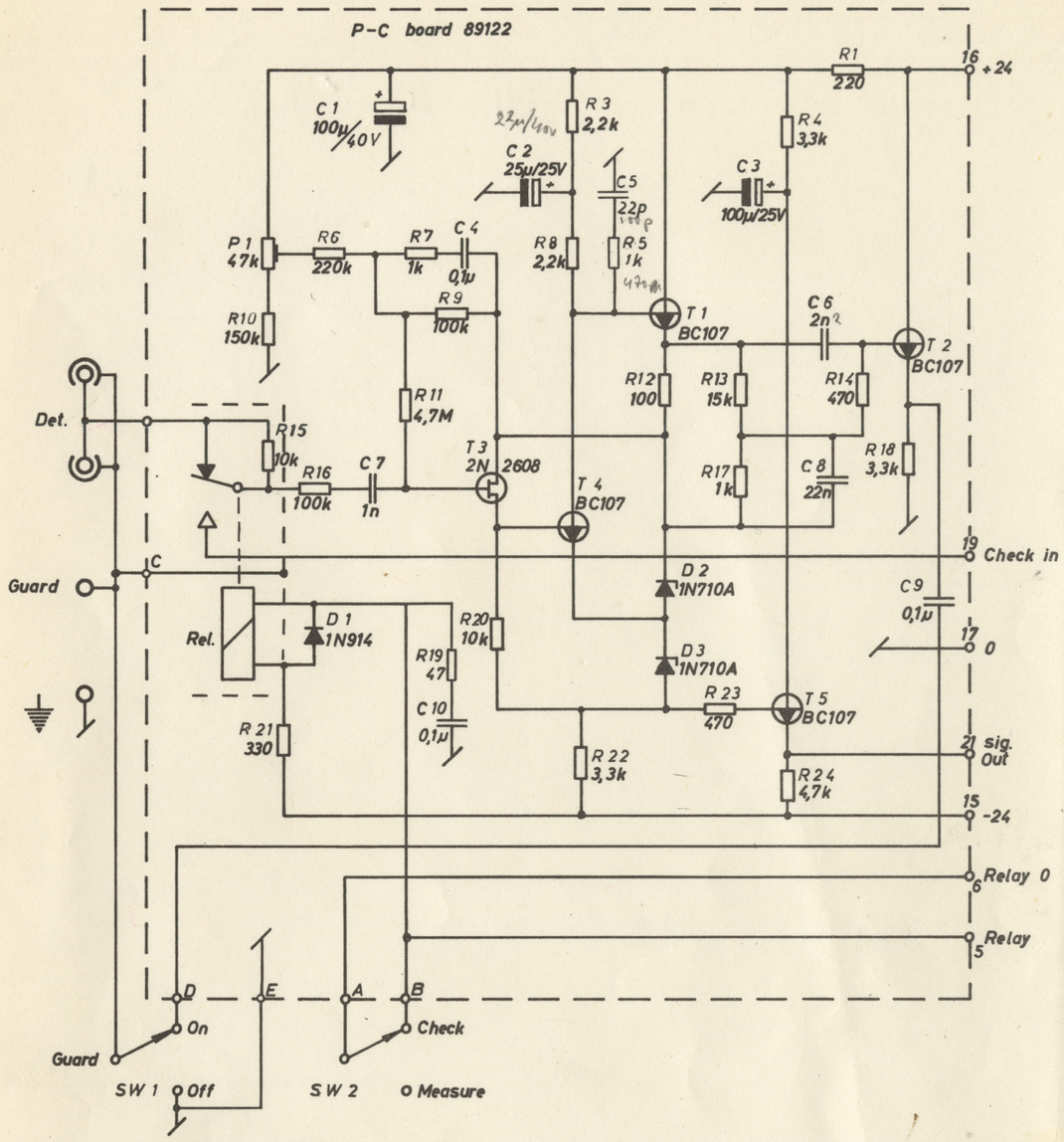
Konstrueret: V. Jensen

Tegnet: [illegible]

Dato: 25-2-70

Godkendt: J.W. Hansen

A/S Danbridge



061272	B.R.				
140471	B.R.				
27-5-70.	B.R.				
020773	B.R.		Rettet d.	Tegn.	Godk.

73622 A

COMPONENT COMPARATOR CPC-4

MODULE CPC-4A1

INPUT AMPLIFIER

CIRCUIT DIAGRAM

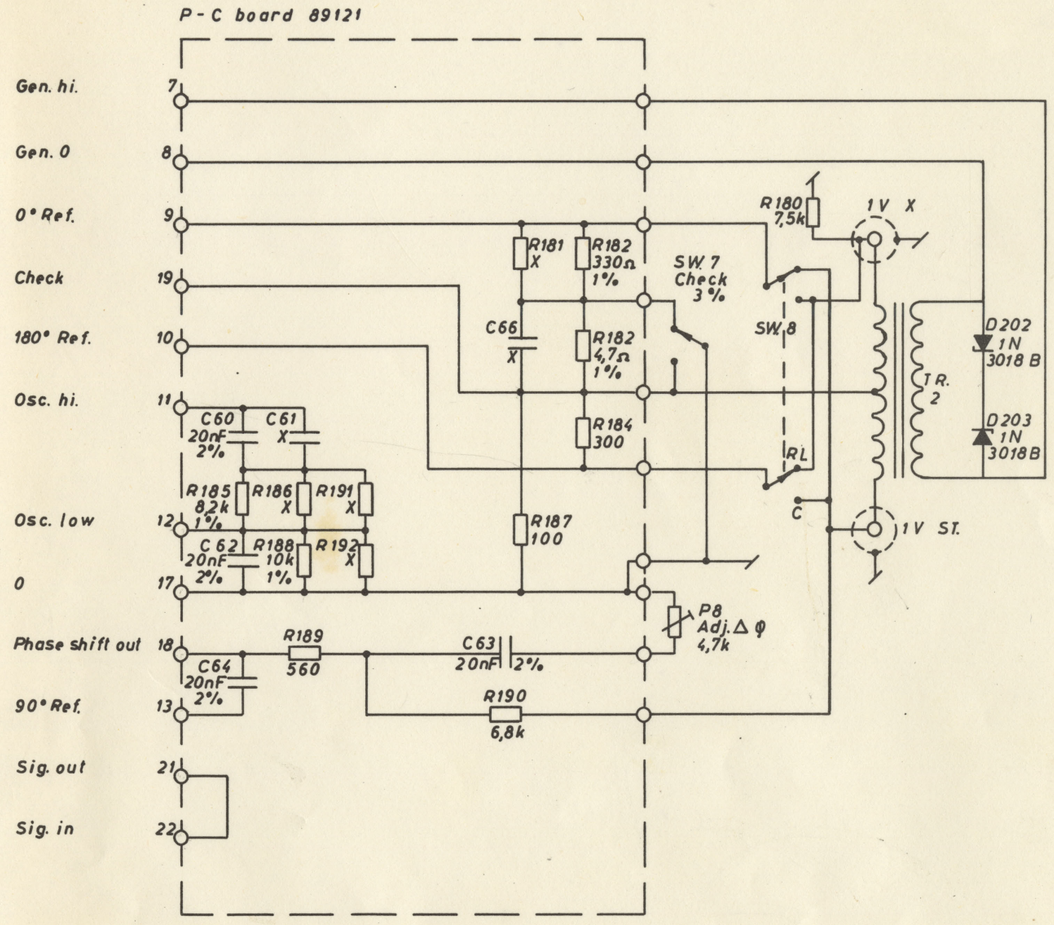
Konstrueret: V. Jensen

Tegnet:

Dato: 25-2-70

Godkendt:

A/S Danbridge



061272	B.R.	
211271	B.R.	
RETTET D.	TEGN.	GODK.

73621

Component Comparator CPC-4

Module CPC-4 B1 1kHz/1V

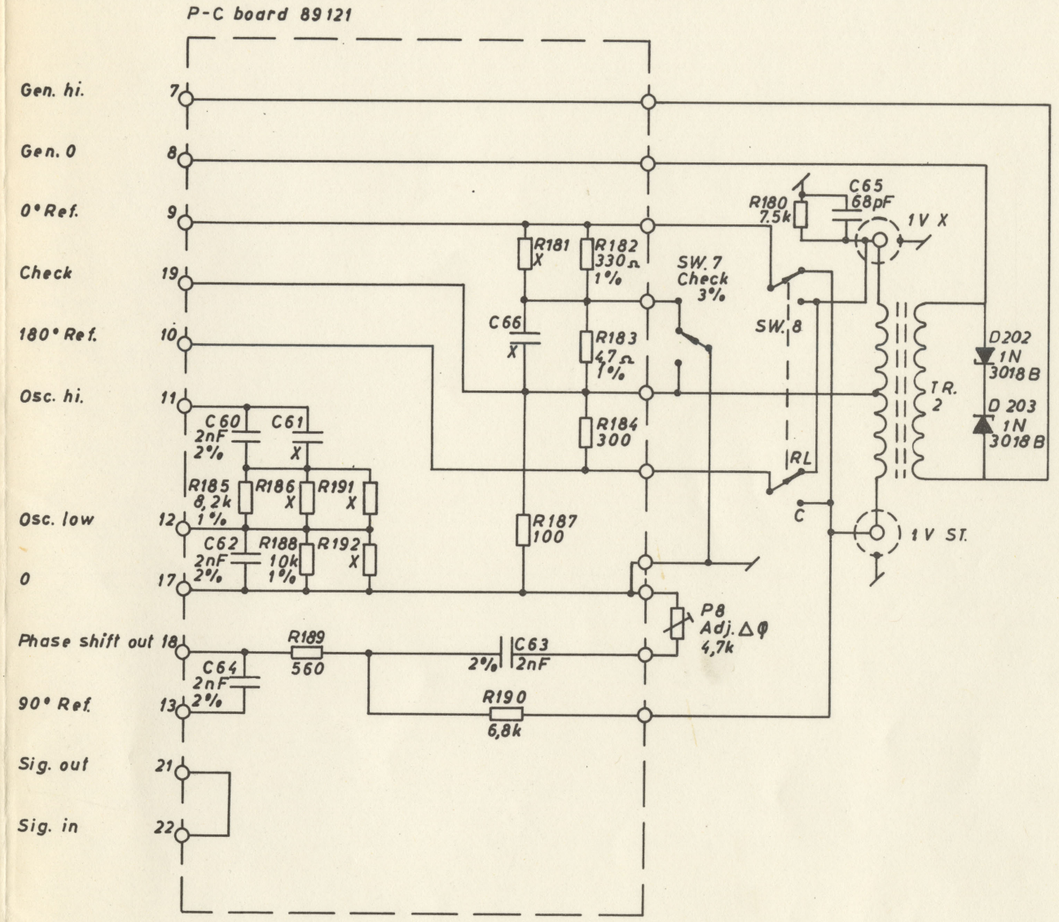
Bridge transformer

Osc. freq. determining circuit

Fase compensating circuit

Konstr.	: V. Jensen
Tegn.	: B. Rasmussen
Dato	: 231170
Godk.	:

A/S Danbridge



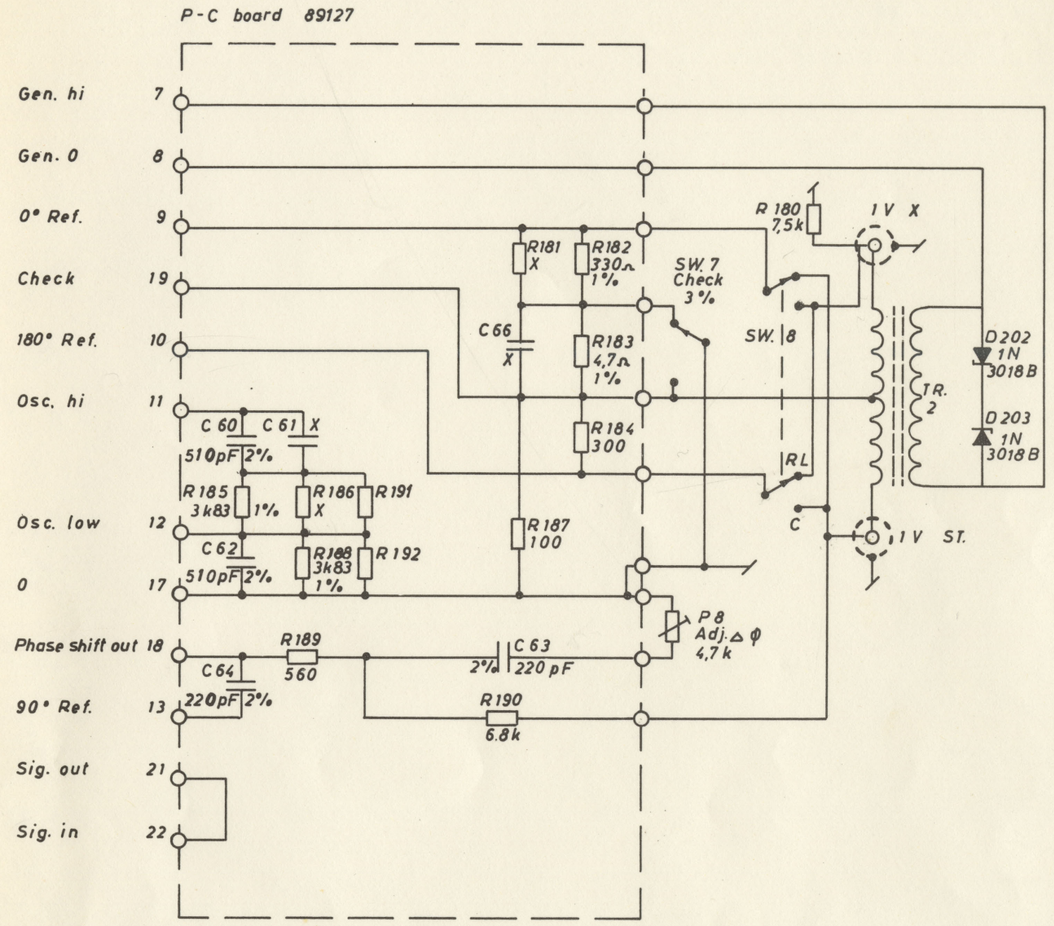
201271	B.R.	
RETTET D.	TEGN.	GODK.

73625

Component Comparator CPC - 4
Module CPC-4 B2 10 kHz / 1V
Bridge transformer
Osc. freq. determining circuit
Fase compensating circuit

Konstr.	: V. Jensen
Tegn.	: B. Rasmussen
Dato	: 201170
Godk.	:

A/S Danbridge



060473	B.R.	
211271	B.R.	
RETTET	TEGN.	GODK.

73626

Component Comparator CPC -4

Module CPC-4 B3 100 kHz/1V

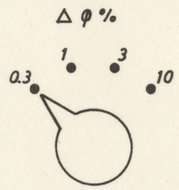
Bridge transformer

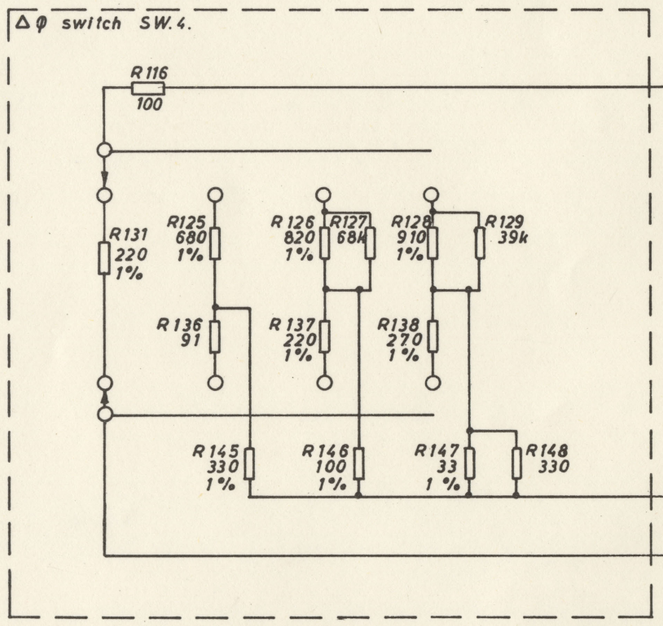
Osc. freq. determining circuit

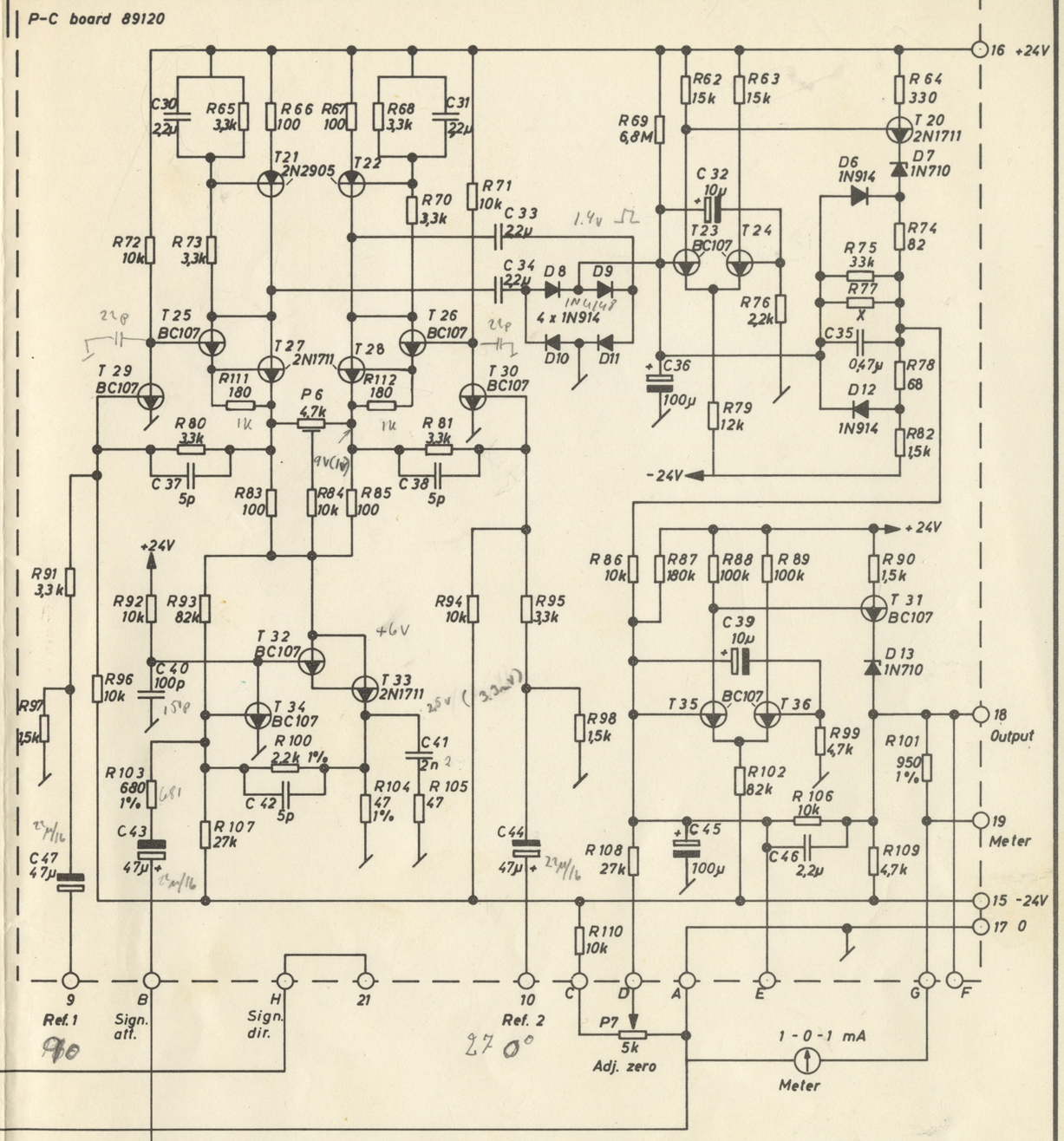
Fase compensating circuit

Konstr	: V.Jensen
Tegn.	: B Rasmussen
Dato	: 221070
Godk.	:

A/S Danbridge







Components marked X are adjusted on test.

190673	B.R.	
200870	B.R.	
27-5-70.	B.R.	
Rettet d.	TEGN.	Godk.

73624

Circuit diagram

Component comparator CPC-4

Modules CPC-4.P1

Phase detector

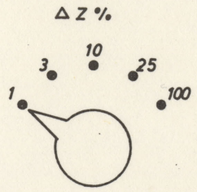
Konstrueret: V. Jensen

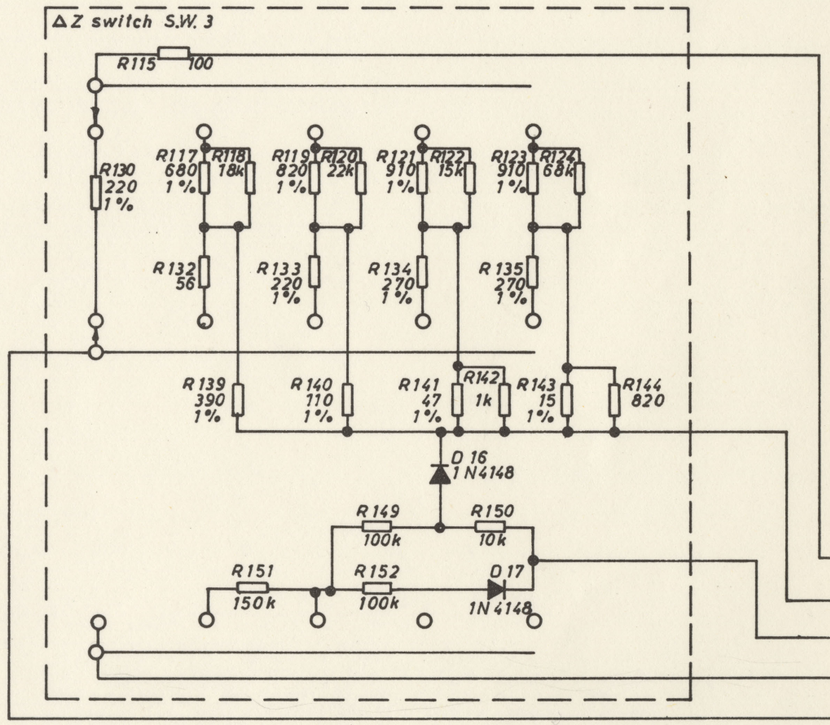
Tegner: Hallmar

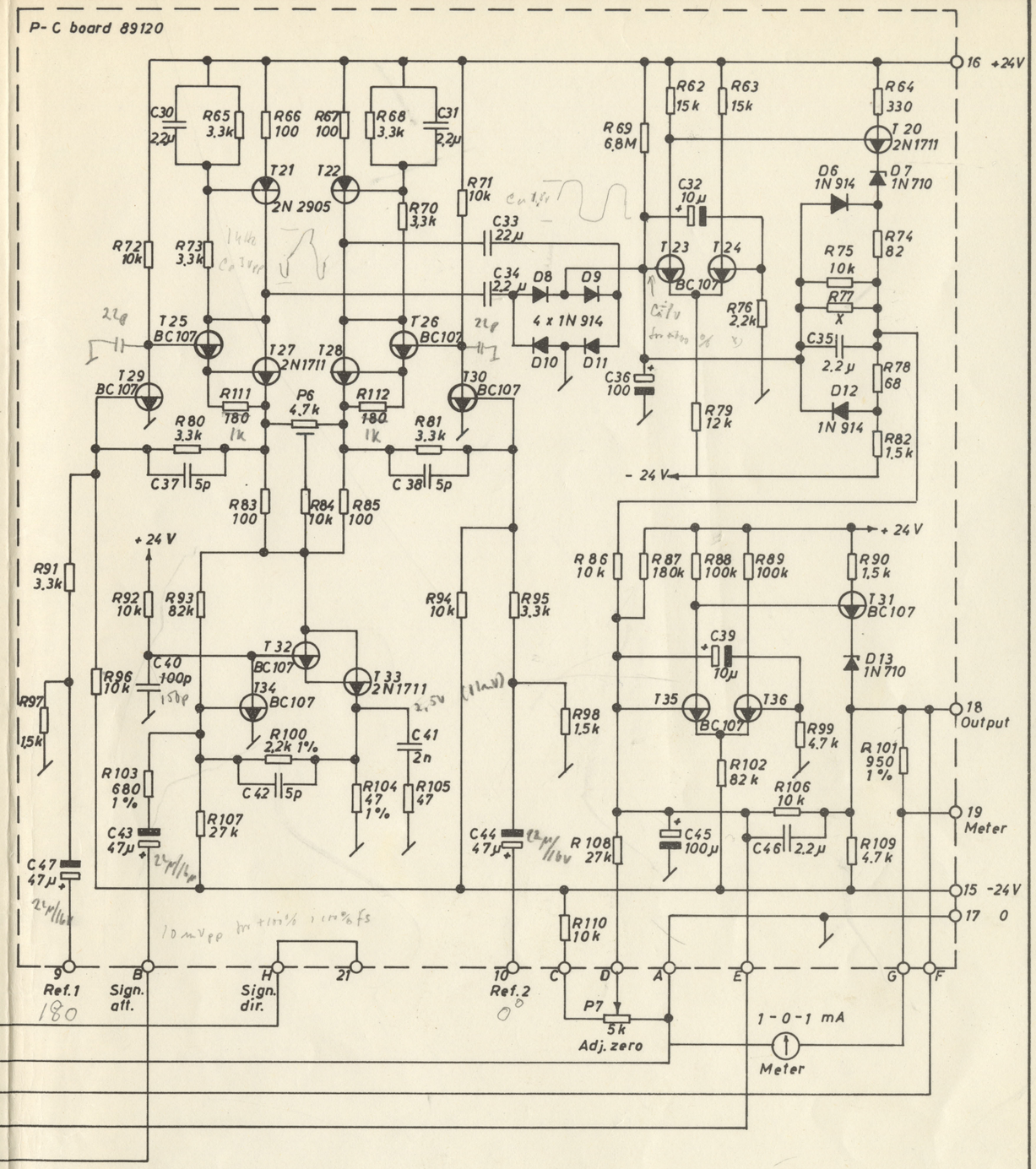
Dato: 24-2-70

Godkendt:

A/S Danbridge

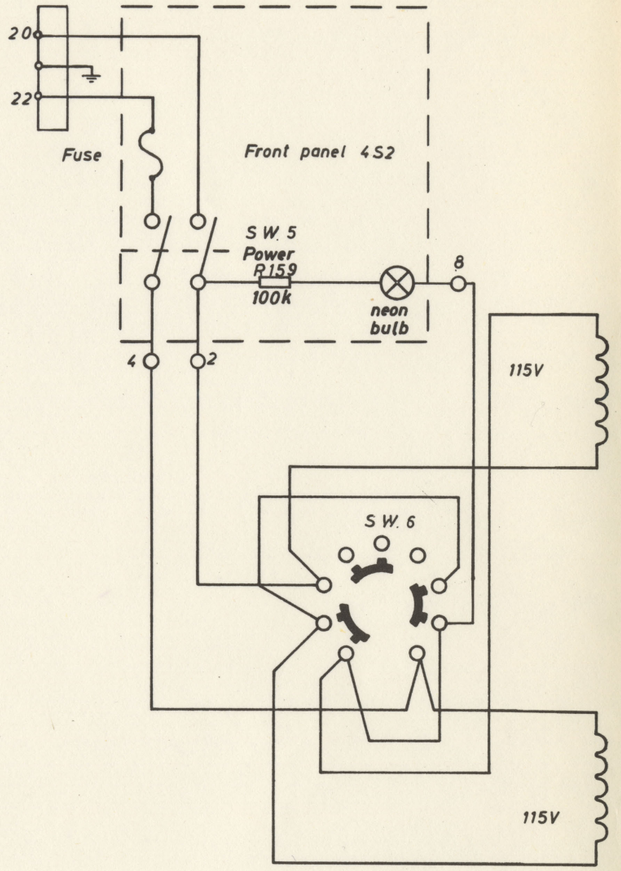






Components marked X are adjusted on test

73623	Circuit diagram	Konstrueret: V. Jensen
	Component comparator CPC-4	Tegner: B. Rasmussen
	Modules CPC-4Z1	Dato : 210673
	Phase detector	Godkendt :
		A/S Danbridge



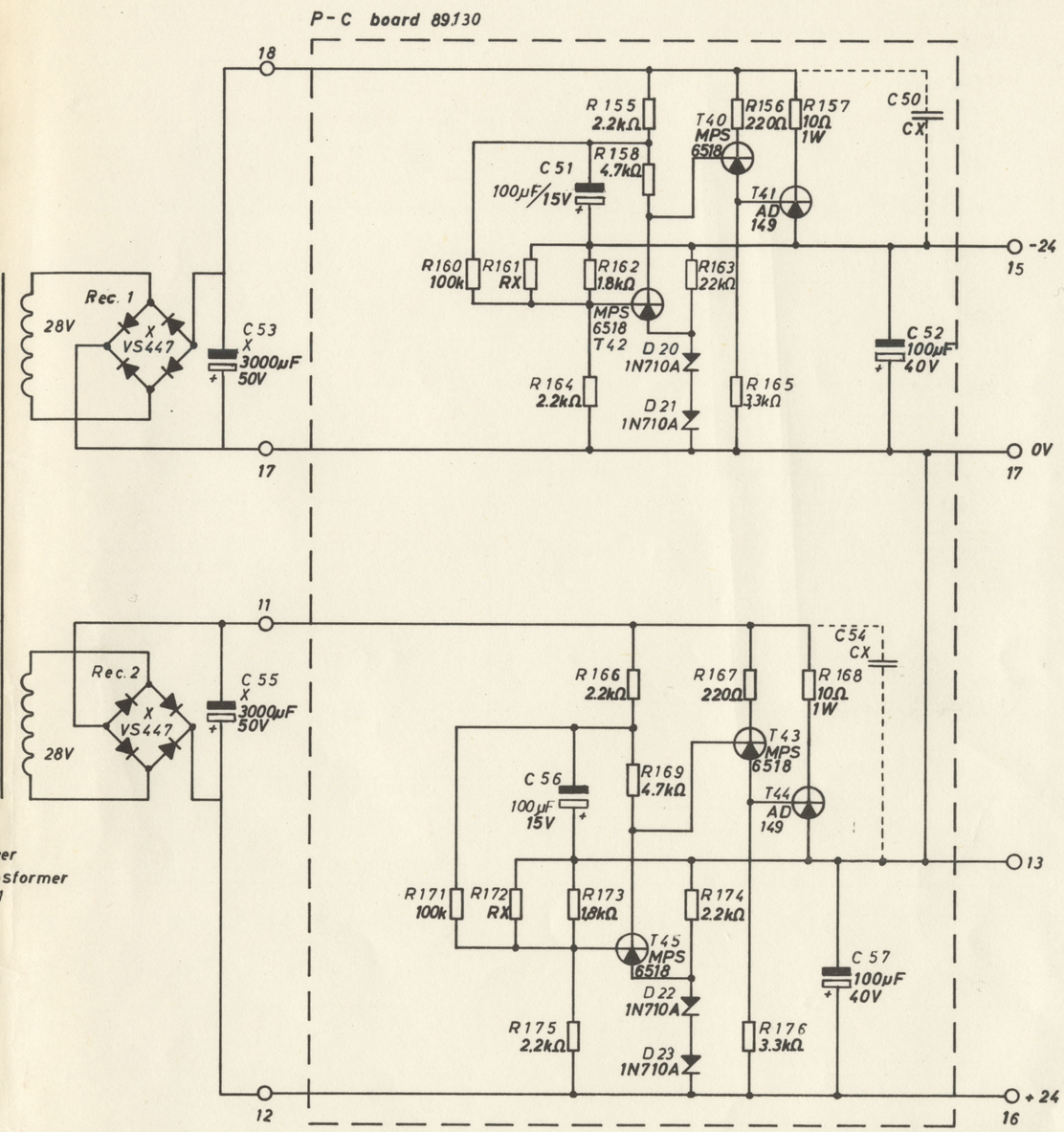
X

Line Voltage Selector
200 - 260V~ / 100 - 130V~

Components marked X
on main frame.

X

Power
transformer
TR. 1



			190173	B.R.	
			071272	B.R.	
			111270	B.R.	
190373	B.R.		27-5-70.	B.R.	
RETTET	TEGN.	GODK.	Rettet d.	Tegn.	Godk.

73628

Component Comparator CPC-4

Module CPC-4S2

Power supply

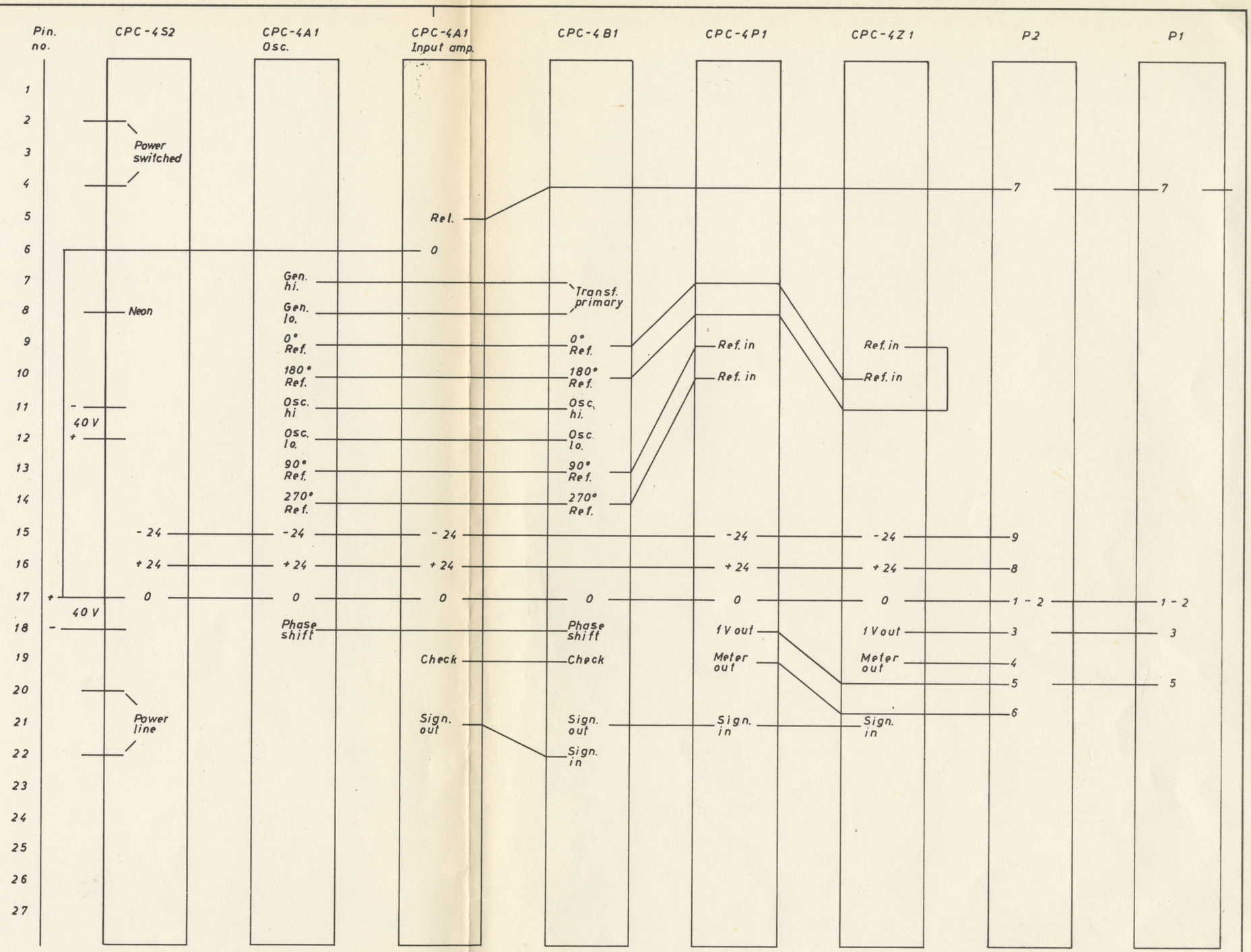
Konstrueret: V. Jensen

Tegner:

Dato: 25-2-70

Godkendt:

A/S Danbridge



190673	B.R.	
190373	B.R.	
190173	B.R.	
061272	B.R.	
RETTET	TEGN.	GODK.

73601

Interconnection wiring between connectors

(seen from rear of cabinet)

Konstr.	: V. Jensen.
Tegn.	: B. Rasmussen.
Dato	: 081270
Godk.	:

A/S Danbridge

4. TLS 1 CIRCUIT DESCRIPTION.

The TLS 1 consists of:

Main Frame TLS 11
Power Module TLS 1M1 (on the rear)
Preamplifier and Regulator Module TLS 1S1
Limit Modules TLS 1L1 (up to 13).

4.1. TLS 1L1 LIMIT MODULE.

Reference: Circuit diagram No. 3

The Limit Module consists of two parts:

The Comparator and the Relay Circuit.

a. The Comparator

is a high-gain integrated amplifier without frequency compensating circuits. The supply voltage is ±15 volt from the reference voltage regulators in the TLS 1S1.

The reference voltages are also supplied to the 10-turn front panel potentiometer (5 KΩ) through 5 KΩ resistors. Thus the potentiometer is a variable voltage divider which set the voltage of the non-inverting input of the comparator between ±5 volt referred to system ground.
The inverting input is connected to the signal output from the pre-amplifier, where the input signal (analog output from the CPC 4) is inverted and amplified 5 times.
The comparator compares the signal input to the voltage set by the 10-turn potentiometer and due to the high-gain and a slight positive feedback the comparator will be in upper or lower saturation in accordance with the signal input being above or below the potentiometer voltage (the limit). The positive feedback gives a small hysteresis of about 2 mV referred to input. The comparator output (saturation) voltage is + or -12 volt referred to ground.

b. The Relay

The relay part consists of a SCR which drives the relay coil, and the SCR gate driving circuit connected to the comparator output. The cathode line of the SCR is either switched to ground or to the minus side of the 12 volt supply by a control relay in the TLS 1S1 module. +12 volt is connected to the anode through the relay coil.
When the cathode line is on ground (the "read" period) the 12 volt circuit is open, and the relay cannot be energized. When the cathode line is on the minus side of the floating 12 volt DC supply (the "display" period), it is at the same time on +15 V referred to ground, apart from a single 1.5 KΩ resistor from the cathode line to +15 V reference. Thus,

during the read period (the SCR cathode line on ground), a 14 volt output from the comparator charges the 0.1 µF capacitor through the diode and the 12 KΩ resistor, but it cannot trigger the SCR because the anode circuit is open. In the display period when the SCR cathode line is switched to -12 volt the capacitor discharges through a 22 KΩ resistor and the SCR gate and the SCR trigger as it has now anode voltage. At the same time the cathode line is on +15 volt, and the gate circuit is disconnected from the comparator, because the diode is reverse biased. The capacitor thus "remembers" the high state of the comparator during "read" period till "display" state and makes the relay draw in the latter state. The SCR will keep the relay energized during the display period. In case the comparator has a low output the relay will not draw in the "display" period because the capacitor has not been charged during the preceding "read" period.

c. The Relay Outputs

The relay has two sets of shift contact, one for lamp driving and one giving contact closures to the output connector P2 for driving sorting machines, re diagrams 4 and 6. The contacts are connected to the corresponding contacts in the neighbour modules (diagram 4) in such a manner that the output (12 V AC lamp voltage and contact closure) appears on output pins, which correspond to the actual band. The 12 V AC is referred to a common "ZERO" pin (pin 1-2, P1).
The contact closures have also a common reference pin (pin 1-2, P2). Both outputs are floating with respect to system ground (Chassis).
The common contact line is fed through the make contacts of an output relay placed on the channel coding board at the rear of the chassis. This relay is energized during the "display" period, but it is delayed with respect to the limit relays in order to avoid a false output as a result of different time constants of the limit relay coils.
Further the output relay has a shift contact, the "ready contact", floating with respect to chassis, which gives two contact closures during a cycle: During "display" period to the make contact - during "read" period to the break contact.

d. Coding the Limit Modules

The same modules are used as LOW, BAND and HIGH Modules (see page 5 - Notes on Setup) except for certain connections with bumpers on the printed circuit board (diagram 5).
For HIGH Modules the "HIGH REJECT" output signals are carried to the output connectors on separate "HIGH LEADS" and a high module can be followed by a low module in the next (right-hand) module place without any interference between the modules.

The coding is made according to circuit diagram 5, where the 4 possibilities are shown.

ΔZ INPUT:

LOW/PASS 1 is the first (left-hand) module in a row and should be set to the most negative limit.

PASS/HIGH is the last (right-hand) module and should be set to the most positive limit.

BAND Module refers to all modules between the above-mentioned.
In case the setup must be extended the easiest thing to do is to move the LOW/PASS 1 module one place (to the left) or the PASS/HIGH module (to the right) and then plug-in a BAND Module.

ΔΦ INPUT:

As usually only one module is used - only a LOW/HIGH module is shown - but of course a number of modules can operate on the ΔΦ input according to the above for the ΔZ input.

e. Output Signals & Output Sockets

Three output signals from the Limit Modules are available:

The Light Signals
The Lamp Voltages
The Contact Closures.

The front panel lamps indicate whether the input is above or below the limit set with the potentiometer. In a sequence of limits the lamps will only light when the next limit is not passed. Thus the lamps also indicate the Band between two limits.
The lamp display will always show low reject in the "read" period, because all relays are de-energized, but the output relay will cut the common line for contact closures, so no contact closures appear on P2 during the "read" period.

The output sockets P1 and P2 are shown on diagram 6. P1 carries the output voltages and P2 the contact closures.
Pin 1 and 2 are common (reference).
The numbers op. 2 ..... 13 refer to outputs from module places 1 to 13, where place 1 is the far left.
High output 1 carries the HIGH reject signal for the ΔZ PASS/HIGH module no matter where the module is placed.
High output 2 carries the HIGH reject signal for the ΔΦ LOW/HIGH module.

4.2. TLS 1S1 REGULATOR AND PREAMPLIFIER MODULE.

This module consists of three parts:

The Preamplifier - diagram 2
The Reference Supply - diagram 1, and
The Control Circuit - diagram 1.

a. Preamplifier

The preamplifiers are mounted on a separate PC-board and consist of two integrated amplifiers. The feed-back resistors set the gain to approx. 5 and the input resistors the input impedance to 10 KΩ.

b. Reference Supply

The ±15 V reference voltages are using 2 integrated regulators placed on the main board together with associated discrete components. The regulators are current limited to approx. 150mA.

c. Control Circuit

the time control circuit is supplied with the 12 V DC unstabilized. The circuit consists of an astable multivibrator which drives the control relay.
The relay has two shift contact sets, one for switching the cathode line of the SCR in the Limit Modules between ground and -12 V DC, and one to control the triggering of the multivibrator. The trigger circuit consosts of a unijunction transistor and a RC circuit connected to the emitter of this transistor. The output pulse of the unijunction transistor is fed to one or the other side of the multivibrator via one relay contact set. The resistors in the RC network are branched through a diode AND-gate and variable resistors to both sides of the multivibrator. Thus the charging currents can be varied independently and thereby the 'on' and 'off' times of the relay. One of the charging paths can be disabled by a switch, whereby the multivibrator will be monostable with the relay de-energized as the stable state ("display" period , because the 12 V DC supply is connected to the limit modules). In this mode the "read" cycle is triggered either by the push-button or by a contact closure between pin 12 and 14 on output socket P2. In the latter case the "read" time will be contact time plus a delay set by the front panel trimpot. between approx. 1 Sec. and a minimum corresponding to the 'on' time for the astable operation.

4.3. TLS 1M1 POWER MODULE

Refer to circuit diagram No. 8.
The Power Module is rearmounted in the main frame and consists of the power transformer, the line voltage selector and the fuse (0.3 A at 230 V AC and 0.5 A at 115 V AV slow blow).

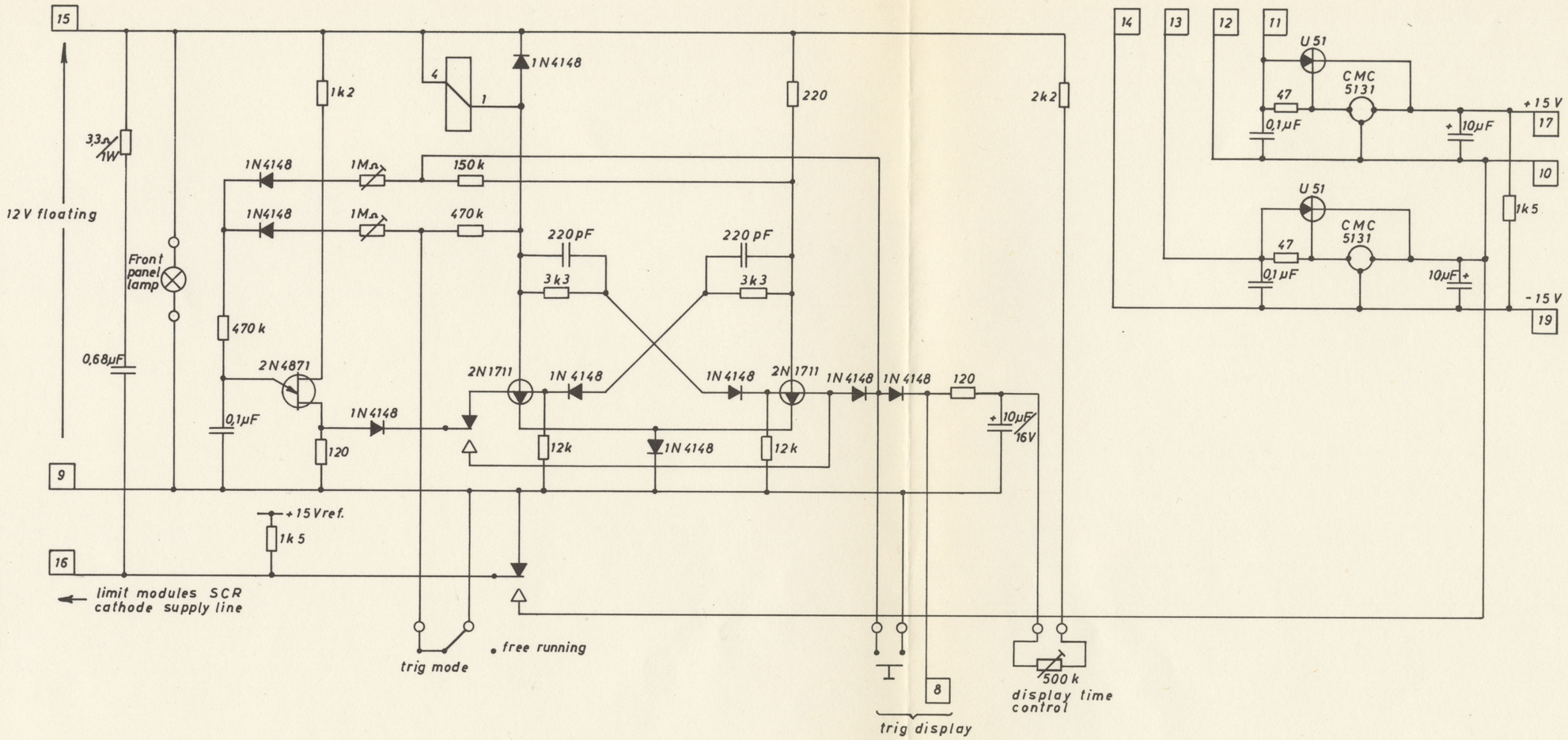
The printed circuit board carries the line voltage through the connectors to the front panel power switch and back to the transformer primary. On the PC-board are mounted also the diode bridges and the electrolytics for the DC voltages.

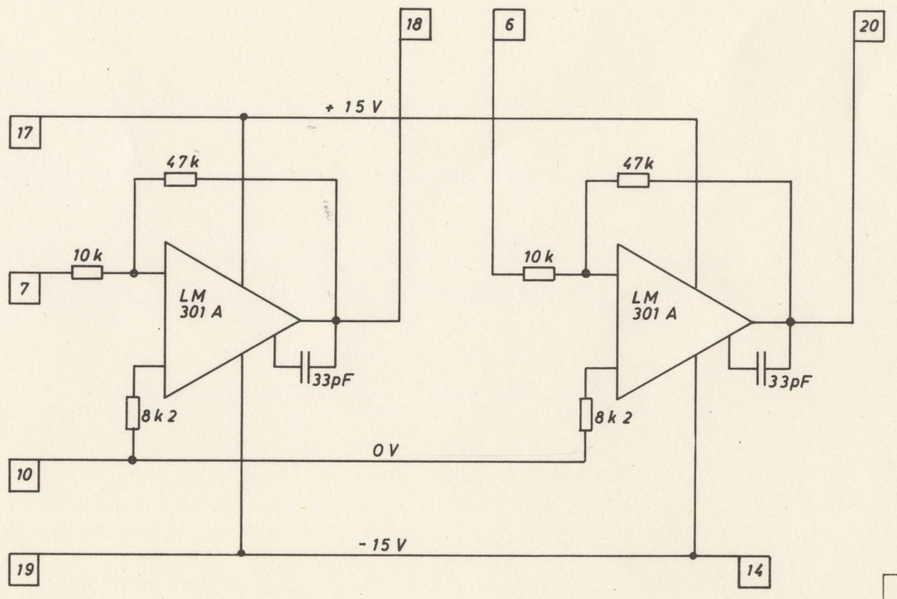
4.4. CHANNEL CODING BOARD.

Refer to diagram 7.
The channel coding board is placed in the rear of the cabinet and is accessible when the top cover and the rear panel

(with output sockets) have been removed. The board enables the TLS 1 Band System (see page 6) to operate as a Channel System, as a channel in effect consists of two bands.

The change to a channel system is obtained by parallelling the outputs of the corresponding bands. The diagram shows the board seen from the rear. For practical reasons the center channel must be between module places 6 and 7, so the output from module place 7 is not fed through the board.
The diagram shows some examples of connections for different number of channels.





1	220 V ~
2	220 V ~
3	220 V ~
4	220 V ~
5	NC
6	Input △ φ
7	Input △ Z
8	Trig
9	-12 V
10	Stel
11	+20 V a
12	-20 V a
13	+20 V b
14	-20 V b
15	+12 V
16	Modul stel
17	+15 V
18	△ Z
19	-15 V
20	△ φ

151272	B.R.	
RETTET	TEGN.	GODK.

93440

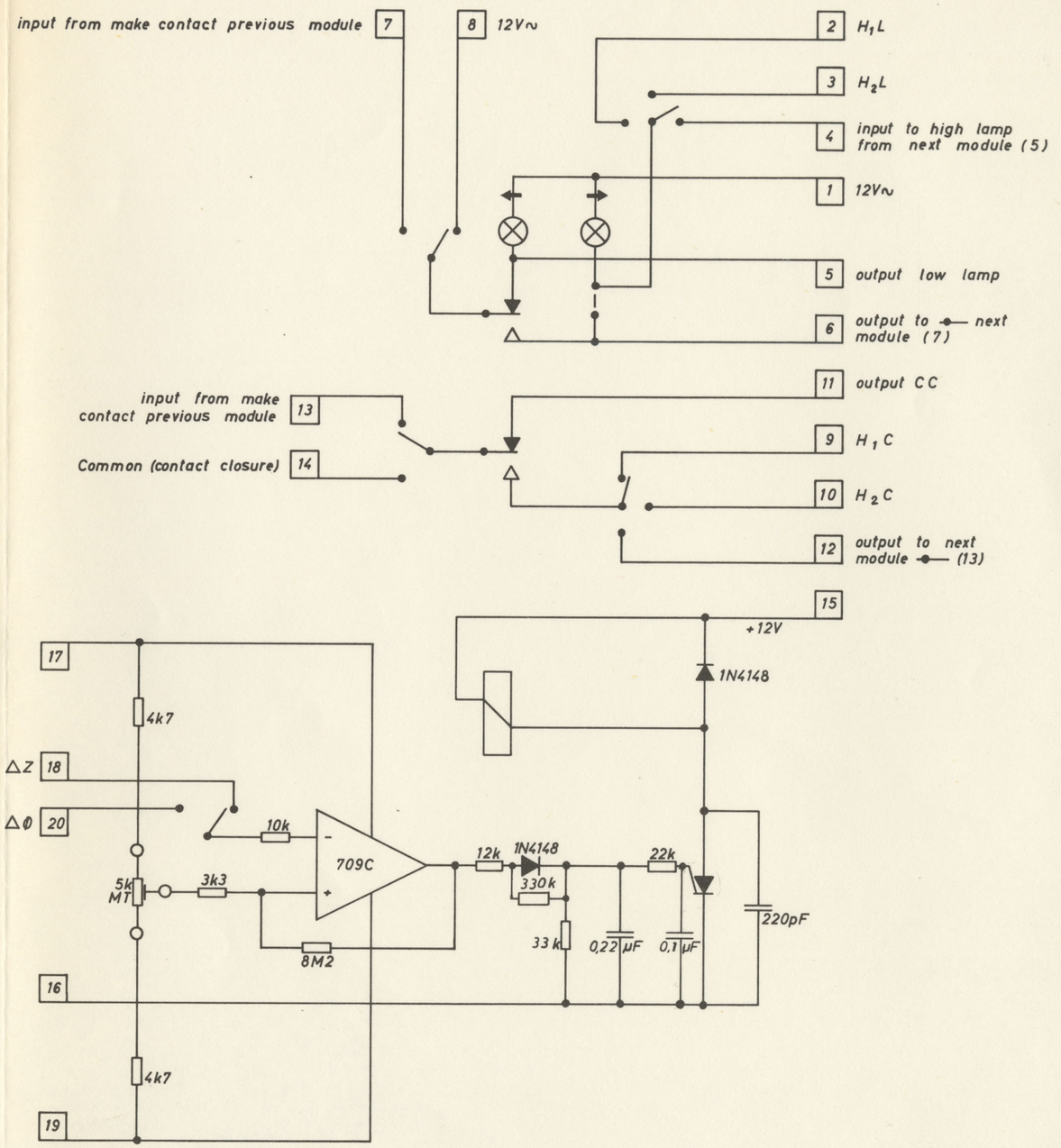
Circuit diagram TLS – 1S1

Print 89102 A

Power supply (± 15 V) time control and dual premplifier

Konstr. :	J.W. Hansen.	
Tegner :	B. Rasmussen.	B.R.
Dato :	191070	151270
Godk. :	J.W. Hansen	

A/S Danbridge



151272	B.R.	
221070	B.R.	
Rettet d.	Tegn.	Godk.

93441-3

Circuit diagram 3

TLS-1L1

Print 89101

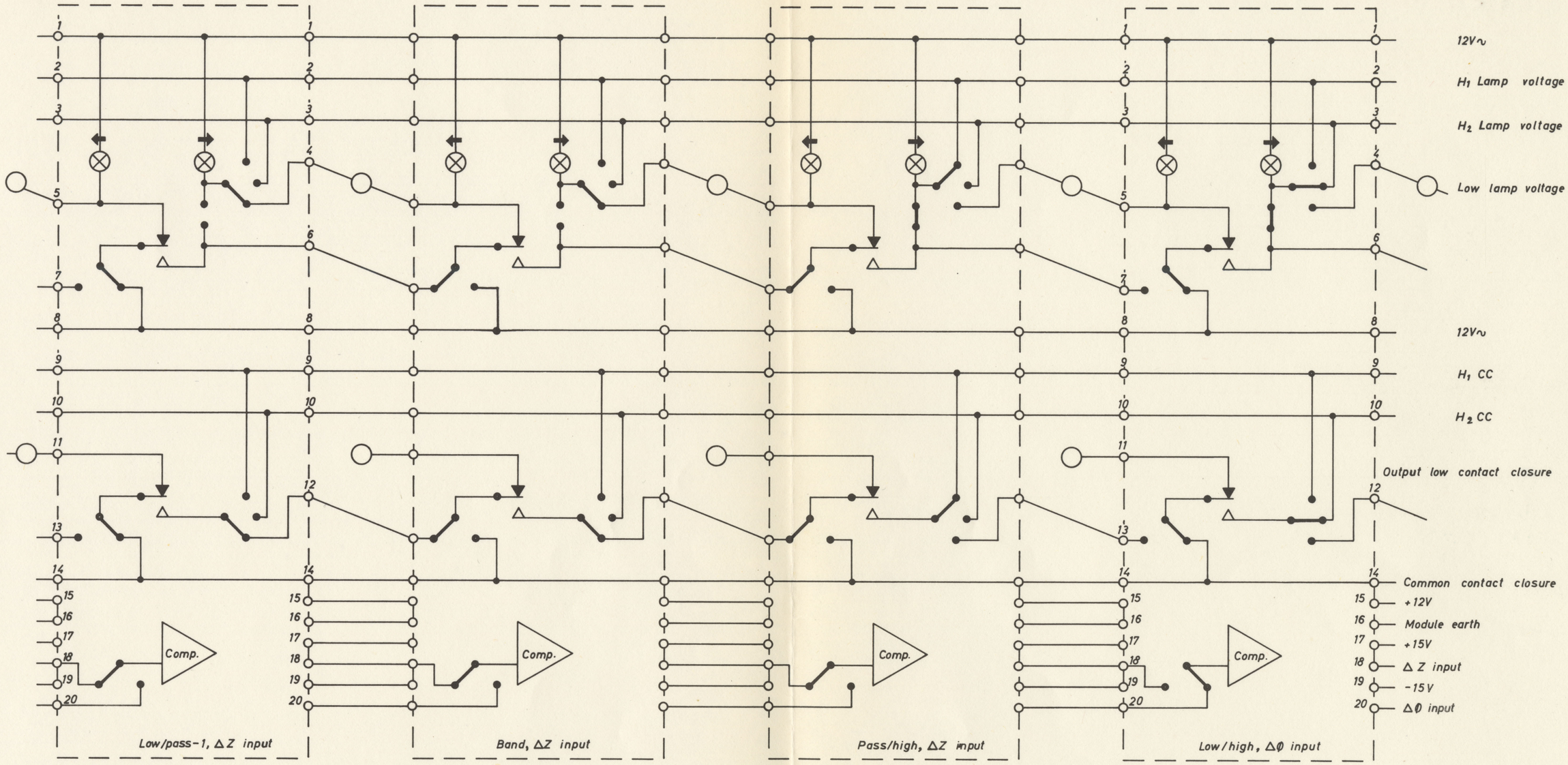
Konstrueret: J.W. Hansen

Tegner:

Dato: 16-12-69

Godkendt:

A/S Danbridge



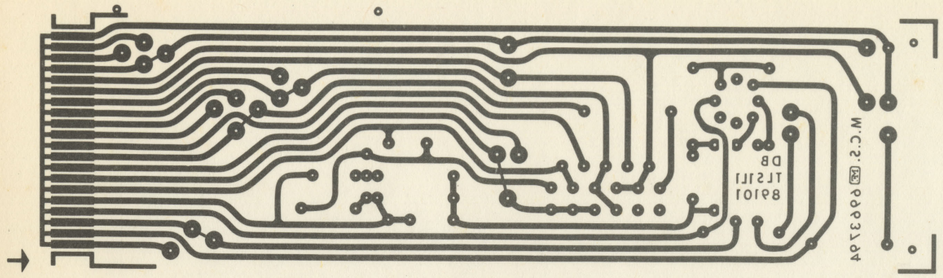
151272	BR.	
RETTET	TEGN	GODK.

93470-4 Circuit diagram 4

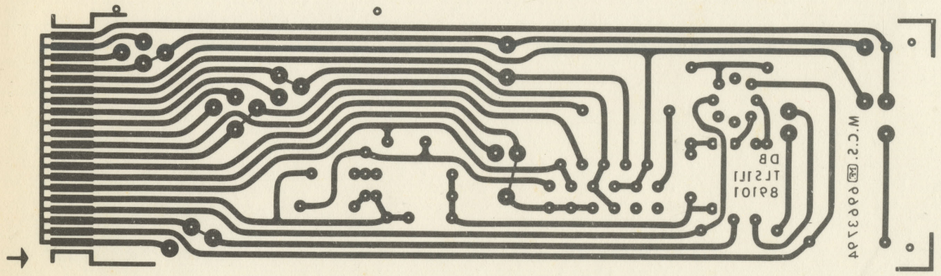
TLS-1
Low-Pass-High-Δ∅ modules
Functional diagram

Konstrueret: J.W. Hansen
Tegner: Holdvar
Dato: 18-12-69
Godkendt: J.W. Hansen.

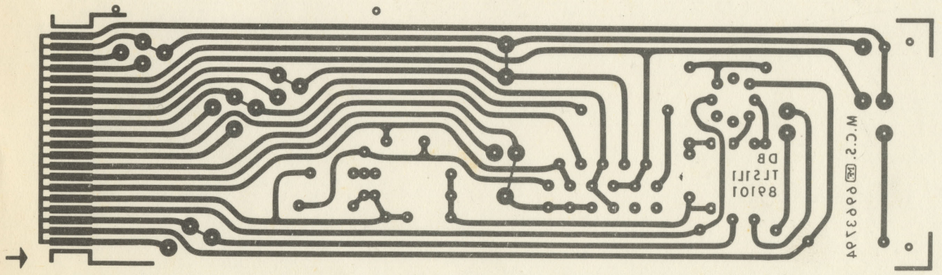
A/S Danbridge



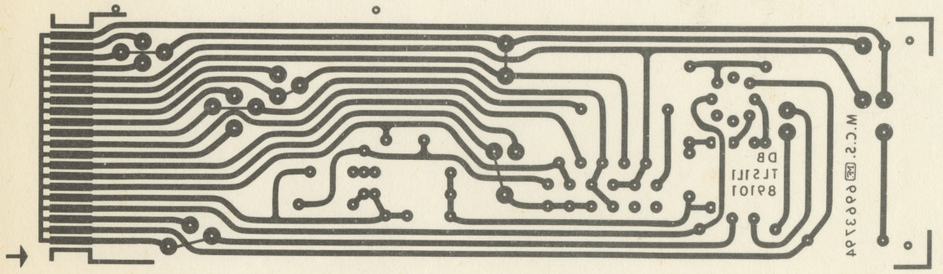
Low/Pass-1. module, ΔZ input



Band module, ΔZ input



Pass/High, ΔZ input



Low/High, $\Delta \varphi$ input

151272	B.R.	
RETTET	TEGN.	GODK.

93441-5

Circuit diagram 5
TLS-1L1
PRINT 89101

Konstr. : J.W. Hansen
Tegn. : B.Rasmussen
Dato : 051170
Godk. :

AS Danbridge

Output Socket P1 Lamp Voltage

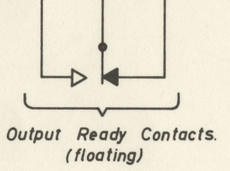
high output 2	high output 1	op. 13	op. 12	op. 11	op. 10	op. 9	op. 8	op. 7	op. 6	op. 5	op. 4	op. 3	op. 2	op. 1	common 12V∿
31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
⊠	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
key	12V∿	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	common 12V∿

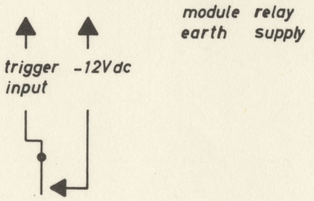
12V∿ (both sides) is floating with respect to TLS-1 ground (case)

Output Socket P2 Contact Closures.

Contact systems are floating with respect to TLS-1 ground (case)

high output 2	high output 1	op. 13	op. 12	op. 11	op. 10	op. 9	op. 8	op. 7	op. 6	op. 5	op. 4	op. 3	op. 2	output 1	common
31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1
⊠	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2
key	●	●	●	NC	NC	NC	NC	NC	○	○	NC	MS	+12Vdc	NC	common





External contact closure to trig 'read' cykle.

NB: The -12Vdc must not be connected to TLS ground.

Input Socket P3

NC	inp. Δϕ	inp. ΔZ	⏚
7	5	3	1
⊠	6	4	2
key	NC	NC	⏚

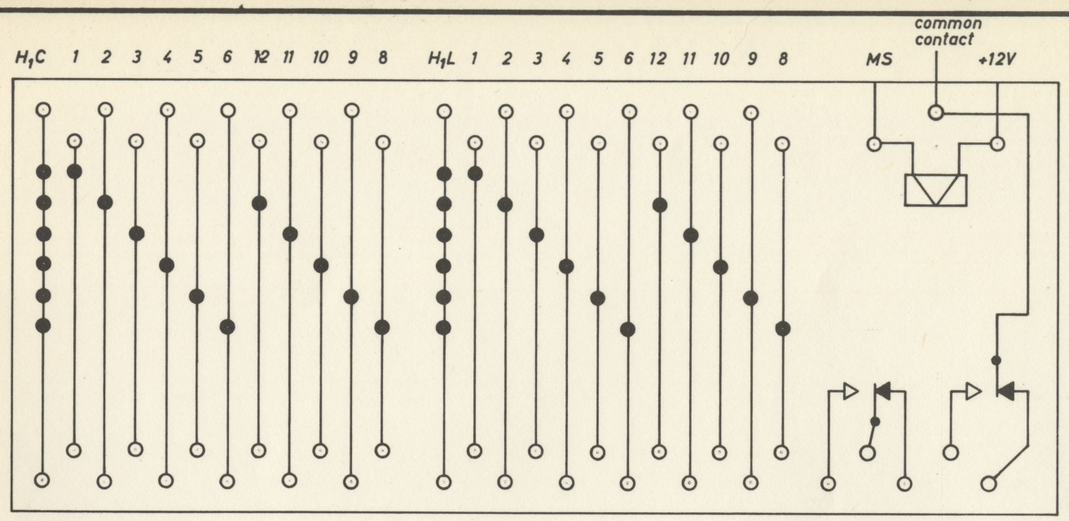
071272 RETTET	B.R. TEGN.	GODK.

93470-6 **Circuit diagram 6**

TLS-1
Output connectors

Konstrueret: J.W. Hansen
Tegner: e.H.Kold.mar
Dato: 23-12-69
Godkendt: J.W. Hansen.

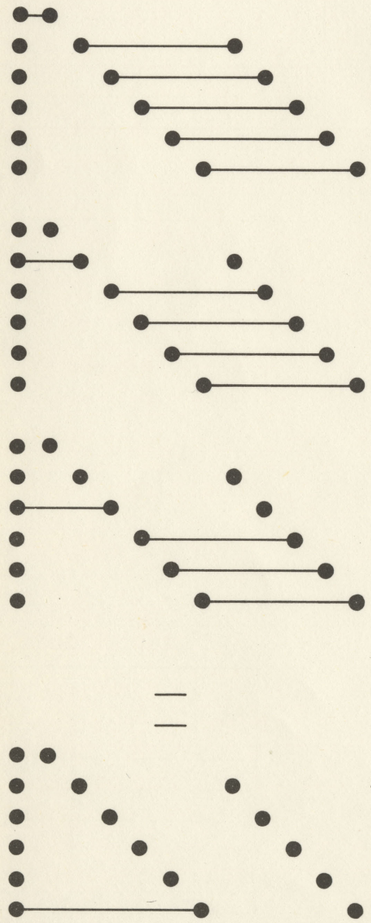
A/S Danbridge



Channel coding board

pin 30 pin 28 pin 26 pin 1-2

'ready' contacts P2



Connections for 6 channel system
(only left part shown, same for right part)
Module place 6-7 giving center ch.

NB: No connections should be made for a band system.

5 channel system

4 channel system

1 channel system

071272	B.R.	
RETTET	TEGN.	GODK.

93470-7

Circuit diagram 7

TLS-1
Channel coding board

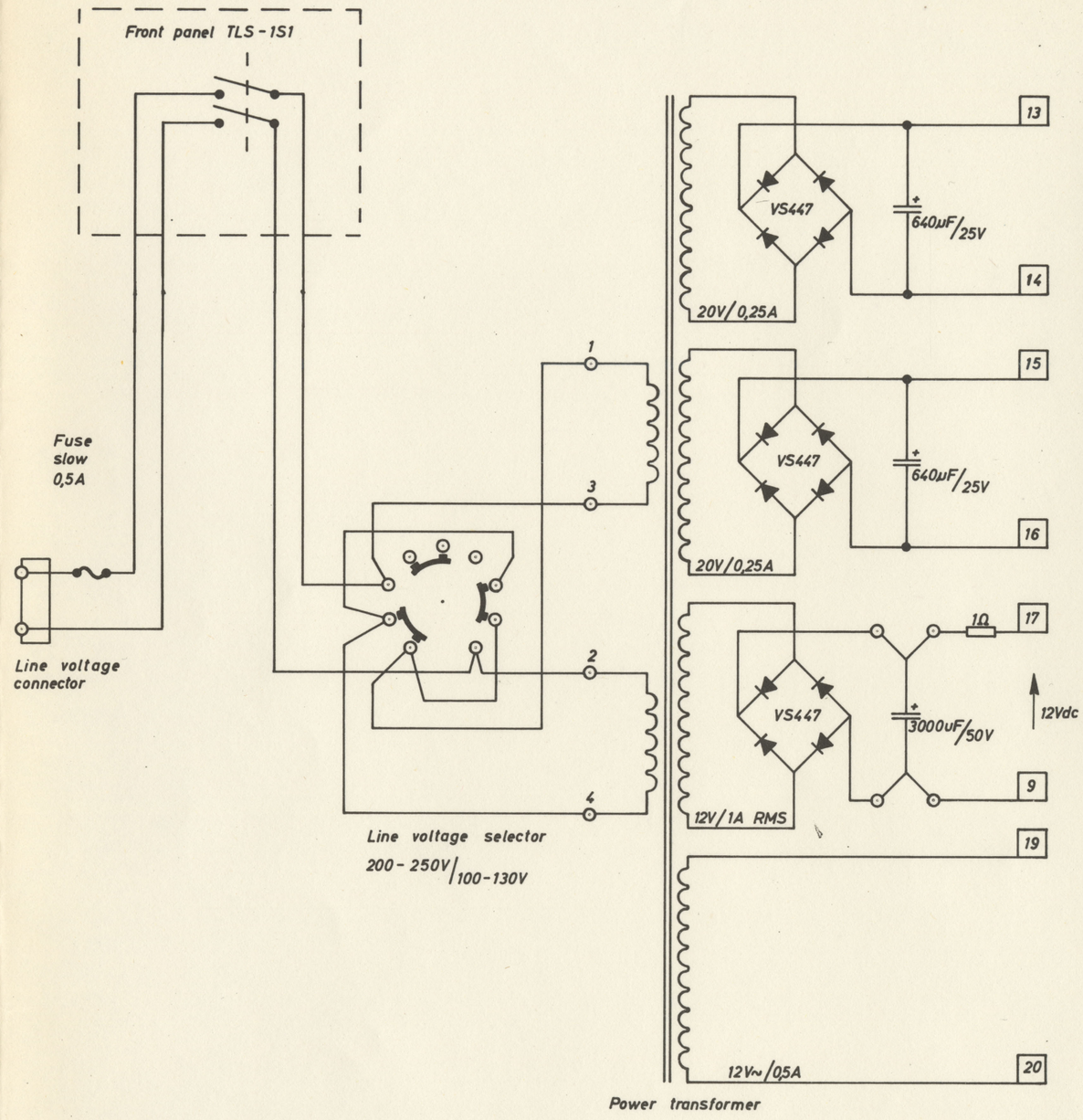
Konstrueret: J.W. Hansen

Tegner:

Dato: 23-12-69

Godkendt: J.W. Hansen.

A/S Danbridge



190173	B.R.	
151272	B.R.	
RETTET	TEGN	GODK.

71007

Circuit diagram 8
TLS-1M1
Power supply module

(mounted in rear of cabinet)

print 89104

Konstrueret: J.W. Hansen

Tegner: H Holdsmar

Dato: 31-12-69

Godkendt: J.W. Hansen

A/S Danbridge